

Proposal for Production Wafer Probing

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Probing up to this time

Requirements for selecting rad-hard “known good die”

Next Steps: Develop specifications for new boards

Wafer Probing as implemented in PixelDAQ

System consists of the following hardware:

- A PLL and PCC, plus a special version of the single chip card acting as a probe adapter card.
- A standard needle-based probe card, plus GPIB-controlled LV supplies and a manual or semi-automatic probe station.

Special software support in PixelDAQ:

- Carry out a pre-defined set of standard tests: record LV supply currents, check HitBus and Test Pixel outputs, check event data output, check chip with digital injection, check chip with coarse analog threshold scan, record all results in files for archiving. Presently no support for automatic wafer stepping.
- This approach allows very thorough test of wafer with 84 good die sites in about 2.5 hours, with constant presence of a person to operate it. In any case, want to perform extra checks whenever a bad die is found.

This approach is very powerful:

- It performs all of the standard tests we would do in the lab, in roughly the same ways that we would do them.
- However, it is not adequate for production probing of rad-hard wafers

Rad-hard Wafer Probing

Problem is fundamentally different:

- Deciding a die is a known good die requires more than just realistic testing under normal operating conditions.
- Need to determine how close the die is to not working properly, by doing more parametric testing of the chip.
- Need to perform tests under more stringent conditions (higher clock frequency or lower power supply voltages) in order to predict that this die will remain a good die after 25 MRad of irradiation.

This requires a testing system which can:

- Perform the same types of tests as now, but also do them at higher clock frequencies than 40 MHz, and vary the timing and amplitude of some of the critical inputs to determine operating margins.
- Gain experience working with irradiated die, where the die have been characterized as a function of supply voltage and clock frequency before irradiation, as well as after. Such correlations are the only way that we can determine what the right “pre-rad” selection criteria are to ensure that the die remain good “post-rad”. Perhaps one hundred die may need to be characterized in this way in order to set final production criteria.

Necessary Hardware

Upgraded or “turbocharged” PLL:

- Need a module which can perform most (if not all) of the functions of the present PLL, and is capable of operating at clock frequencies up to about 100 MHz.
- The entire present PLL is synchronously clocked at the XCK frequency. Speeding up the entire board by a factor of up to 2.5 is not possible without great expense.
- Alternate approach is to insert high-speed FIFOs between the present PLL and the new PCC. The outgoing FIFO would accept data from the PLL at 40 MHz and clock it out at a higher XCK frequency. The incoming FIFO would accept data at the higher XCKR frequency, and would provide it to the PLL at whatever frequency the PLL chose to receive it.

Significantly more powerful version of PCC:

- Must provide ability to vary timing and voltages on output lines, and ability to vary thresholds on input lines, similar to what is done in commercial IC testers.
- There exist chips to do this from Analog Devices. They include programmable delay lines, programmable pin drivers, and programmable window comparators that operate well above 100 MHz.
- LBL is presently designing a card to do this for the SCT wafer probing effort, based on these concepts. It looks like an excellent approach.

Proposal Begin to work on “second generation” PLL:

- Change from present ORCA2C FPGA to more modern ORCA2T array (incompatible packaging technology), allowing significant upgrade in gate count and speed grade. This would provide additional future contingency in the PLL.
- Implement proposed changes by including large, high-speed FIFOs between the FPGA controller and the cable drivers, and upgrading the cable drivers for higher speed.
- The output from the PLL includes 8 lines (STRI, LV1T, DCI, CCKT, RSI, LDT, SYNCT, TM) plus the clock XCK. The input to the PLL includes 3 lines (DTO, CCKR, LDR) plus a return clock XCKR. These fit easily into typical 9-bit wide FIFOs. The output FIFO need not be large but the resync FIFO should be large.
- The PLL software would be changed to add proper control of “bursting out” data from the high speed FIFO output so that atomic operations appeared as contiguous bit streams at the higher XCK frequency.
- The system would be designed to work at up to 100 MHz XCK frequency over the cable, while the PLL itself would not need to operate at speeds higher than 40 MHz. Additional restrictions would no doubt apply to cable length when operating at elevated frequencies. The real XCK would be programmable using a clock synthesizer chip.

Begin to work on “wafer probing” PCC (WPC):

- Implement full programmable control of input and output lines to drive the chip under test. This would include control of low and high voltage levels as well as precise timing on all output lines to the chip under test (STRI, LV1T, DCI, CCKT, RSI, LDT, SYNCT). It would also include use of window comparators on input lines from the chip under test (DTO).
- It would be necessary to connect the chip under test (either mounted on a support card, or contacted by a probe card) to this new card with a very short cable, probably different form what we use today.
- The assumption is that the parameters for these lines would be controlled using the present PCC communication protocol from the PLL. However, further analysis is required to see whether this meets the timing requirements of the various scans that would be performed, or whether a faster mechanism would be needed (which would violate the cable interface from the present PLL and create incompatible boards).
- The whole card would be engineered to run at up to 100 MHz. This should allow us to push the FE chip to its limits. It remains to be seen whether a simple probe card would work well at these frequencies, or whether more expensive membrane probe cards would be needed.

Next Steps

Work out design of proposed improved PLL and new WPC in more detail.

Discuss requirements more carefully with chip designers, then proceed with schematics.

New hardware and software would not be ready for initial FE-D testing (unfortunately), but could be used towards the end of the year to test the last of the FE-D wafers.